

N-Channel Power MOSFET

20V, 3.9A, 65mΩ

FEATURES

- Low $R_{DS(ON)}$ to minimize conductive losses
- Low gate charge for fast power switching
- Compliant to RoHS directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

KEY PERFORMANCE PARAMETERS

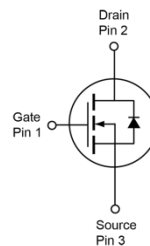
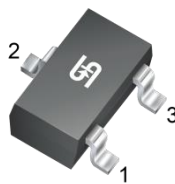
PARAMETER	VALUE	UNIT
V_{DS}	20	V
$R_{DS(on)}$ (max)	$V_{GS} = 4.5V$	65
	$V_{GS} = 2.5V$	95
Q_g	7.8	nC

APPLICATIONS

- Load switch
- Backlights



SOT-23



Note: MSL 3 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 8	V
Continuous Drain Current ^(Note 1)	$T_C = 25^\circ\text{C}$	3.9	A
	$T_A = 25^\circ\text{C}$	3.2	
Pulsed Drain Current	I_{DM}	15.6	A
Total Power Dissipation	$T_C = 25^\circ\text{C}$	1.5	W
	$T_C = 125^\circ\text{C}$	0.3	
Total Power Dissipation	$T_A = 25^\circ\text{C}$	1	W
	$T_A = 125^\circ\text{C}$	0.2	
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150	$^\circ\text{C}$

THERMAL PERFORMANCE

PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	84	$^\circ\text{C/W}$
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	124	$^\circ\text{C/W}$

Thermal Performance Note: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	20	--	--	V
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu A$	$V_{GS(TH)}$	0.65	0.9	1.2	V
Gate-Source Leakage Current	$V_{GS} = \pm 8V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Drain-Source Leakage Current	$V_{GS} = 0V, V_{DS} = 20V$	I_{DSS}	--	--	1	μA
	$V_{GS} = 0V, V_{DS} = 20V$ $T_J = 125^\circ\text{C}$		--	--	100	
Drain-Source On-State Resistance (Note 2)	$V_{GS} = 4.5V, I_D = 3.2A$	$R_{DS(on)}$	--	34	65	m Ω
	$V_{GS} = 2.5V, I_D = 3.2A$		--	45	95	
Forward Transconductance (Note 2)	$V_{DS} = 5V, I_D = 3.2A$	g_{fs}	--	19	--	S
Dynamic (Note 3)						
Total Gate Charge	$V_{GS} = 4.5V, V_{DS} = 10V,$ $I_D = 3.2A$	Q_g	--	7.8	--	nC
Total Gate Charge	$V_{GS} = 2.5V, V_{DS} = 10V,$ $I_D = 3.2A$	Q_g	--	5	--	
Gate-Source Charge		Q_{gs}	--	1	--	
Gate-Drain Charge		Q_{gd}	--	2.5	--	
Input Capacitance	$V_{GS} = 0V, V_{DS} = 10V$ $f = 1.0\text{MHz}$	C_{iss}	--	587	--	pF
Output Capacitance		C_{oss}	--	94	--	
Reverse Transfer Capacitance		C_{rss}	--	64	--	
Gate Resistance	$f = 1.0\text{MHz},$ open drain	R_g	--	1.6	--	Ω
Switching (Note 3)						
Turn-On Delay Time	$V_{GS} = 4.5V, V_{DS} = 10V,$ $I_D = 3.2A, R_G = 2\Omega,$	$t_{d(on)}$	--	5.4	--	ns
Turn-On Rise Time		t_r	--	26.4	--	
Turn-Off Delay Time		$t_{d(off)}$	--	16.4	--	
Turn-Off Fall Time		t_f	--	15.8	--	
Source-Drain Diode						
Forward Voltage (Note 2)	$V_{GS} = 0V, I_S = 3.2A$	V_{SD}	--	--	1.2	V
Reverse Recovery Time	$I_S = 3.2A,$ $di/dt = 100A/\mu s$	t_{rr}	--	19	--	ns
Reverse Recovery Charge		Q_{rr}	--	8	--	nC

Notes:

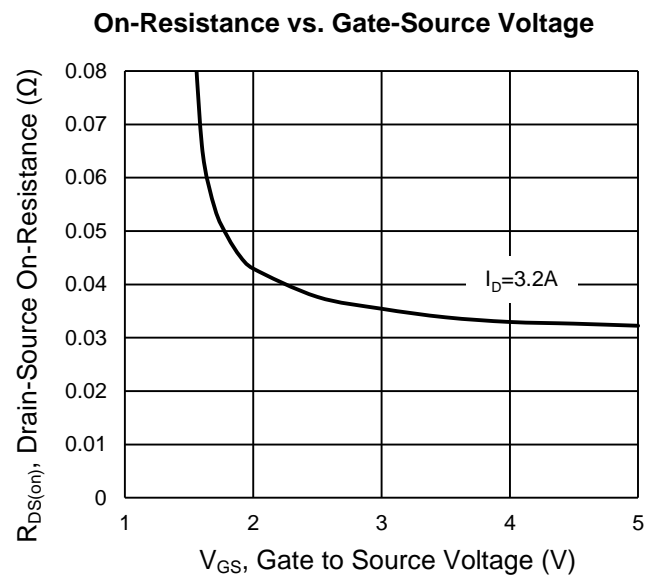
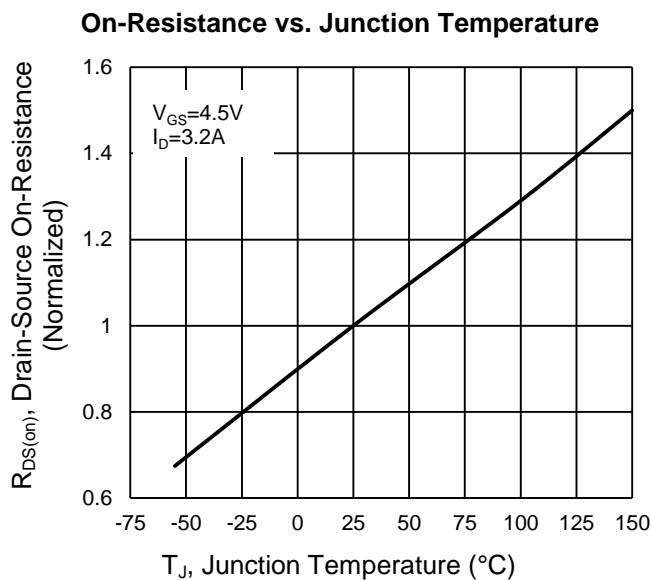
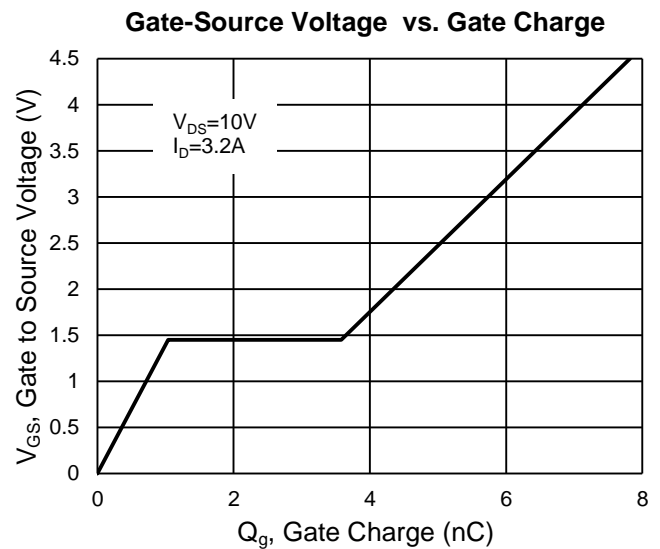
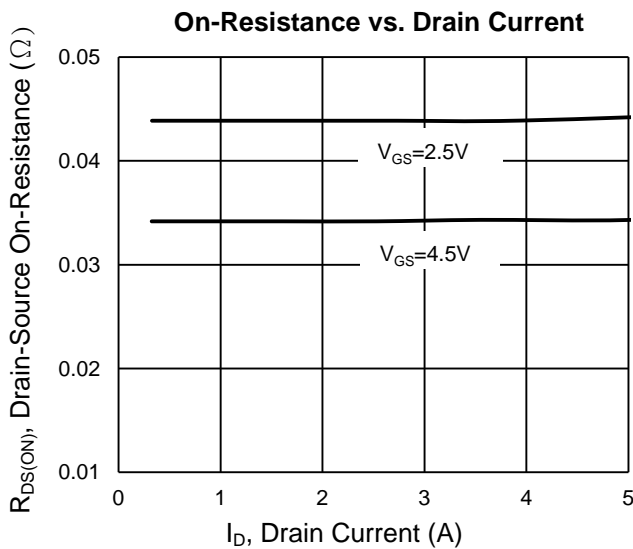
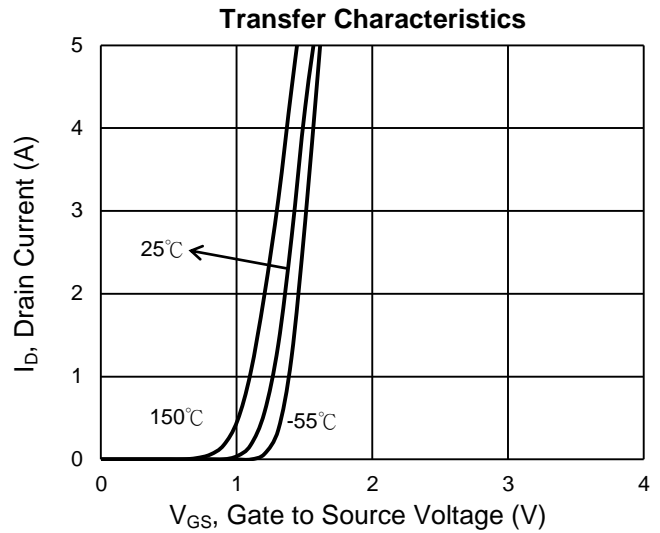
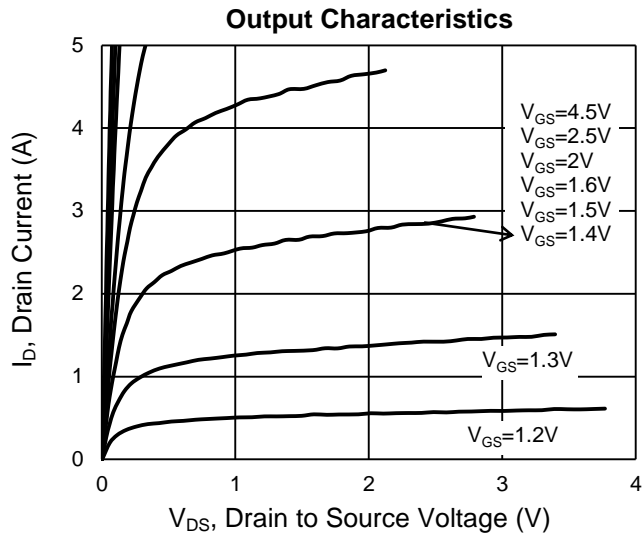
1. Silicon limited current only.
2. Pulse test: Pulse Width $\leq 300\mu s$, duty cycle $\leq 2\%$.
3. Switching time is essentially independent of operating temperature.

ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM2302CX RFG	SOT-23	3,000pcs / 7" Reel

CHARACTERISTICS CURVES

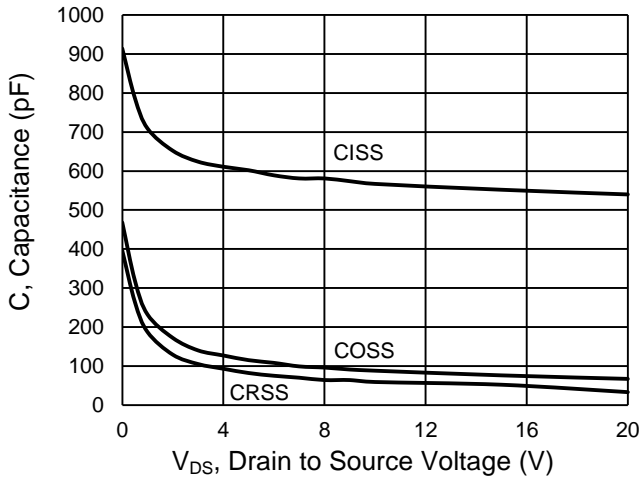
($T_A = 25^\circ\text{C}$ unless otherwise noted)



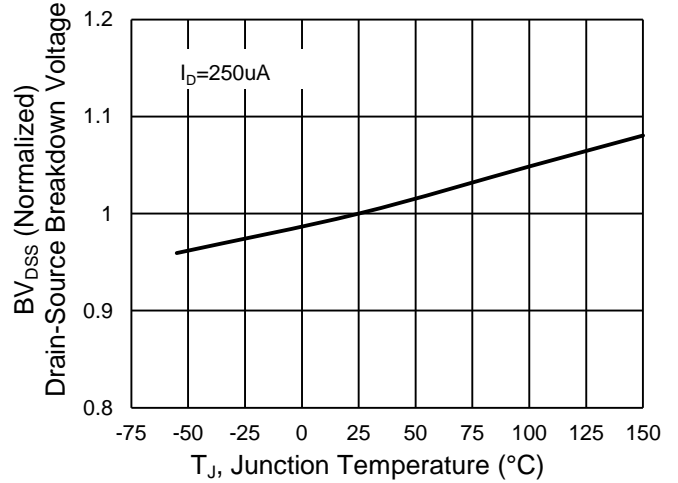
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

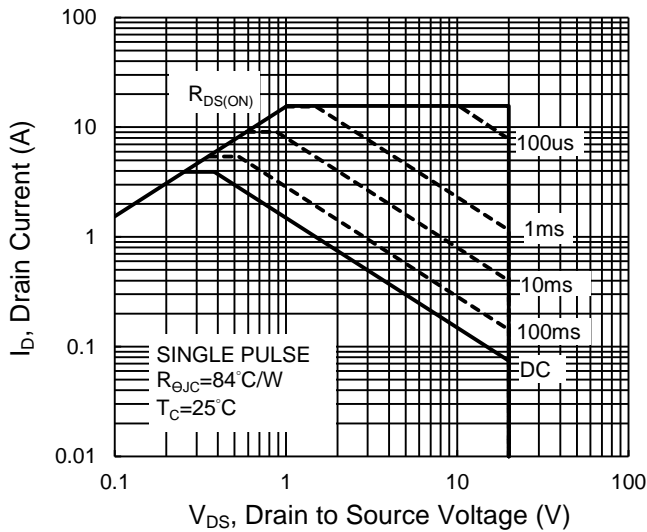
Capacitance vs. Drain-Source Voltage



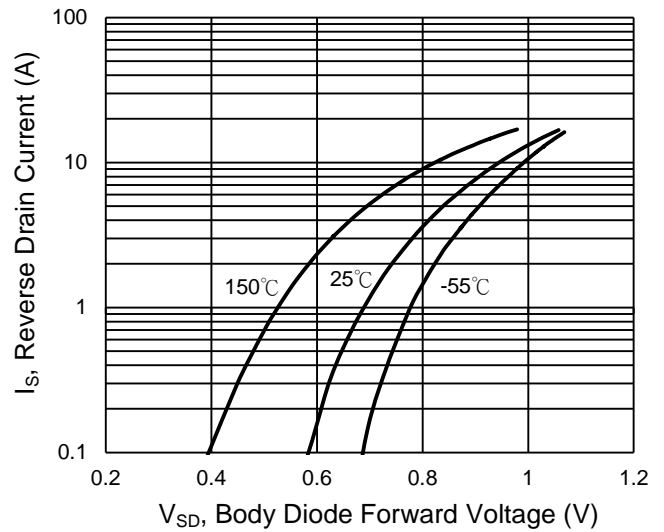
BV_{DSS} vs. Junction Temperature



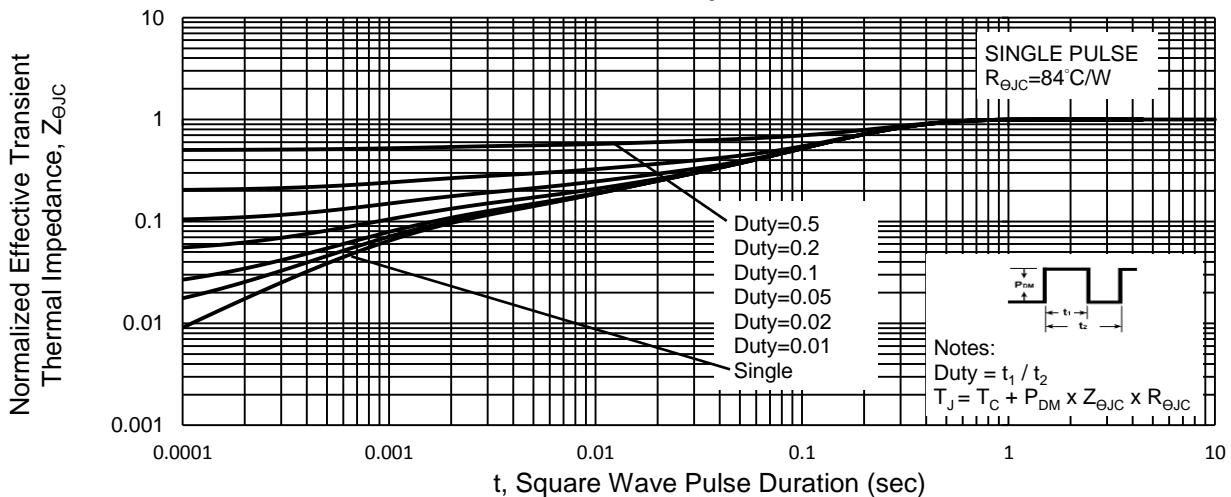
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage

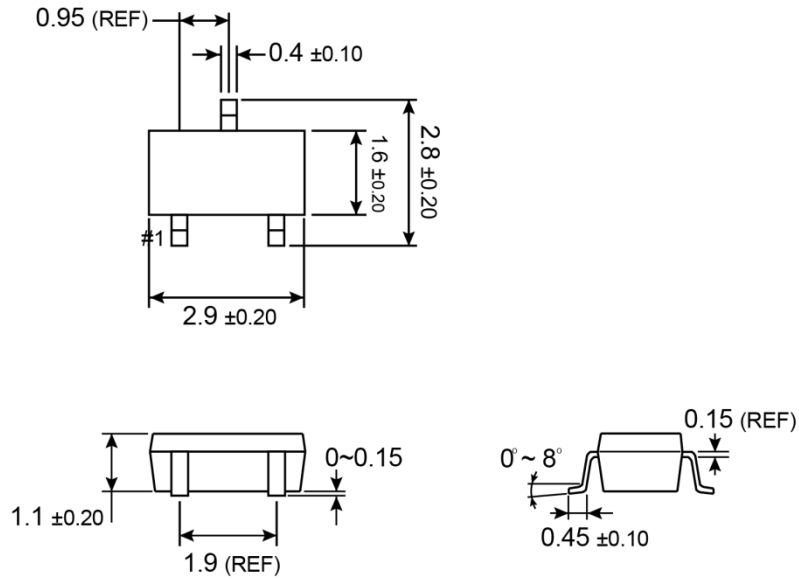


Normalized Thermal Transient Impedance, Junction-to-Case

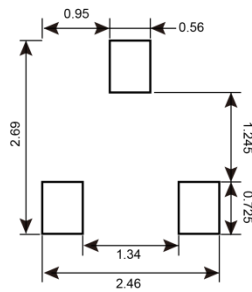


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

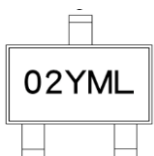
SOT-23



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



- 2** = Device Code
- Y** = Year Code
- M** = Month Code
- O** =Jan **P** =Feb **Q** =Mar **R** =Apr
- S** =May **T** =Jun **U** =Jul **V** =Aug
- W** =Sep **X** =Oct **Y** =Nov **Z** =Dec
- L** = Lot Code

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